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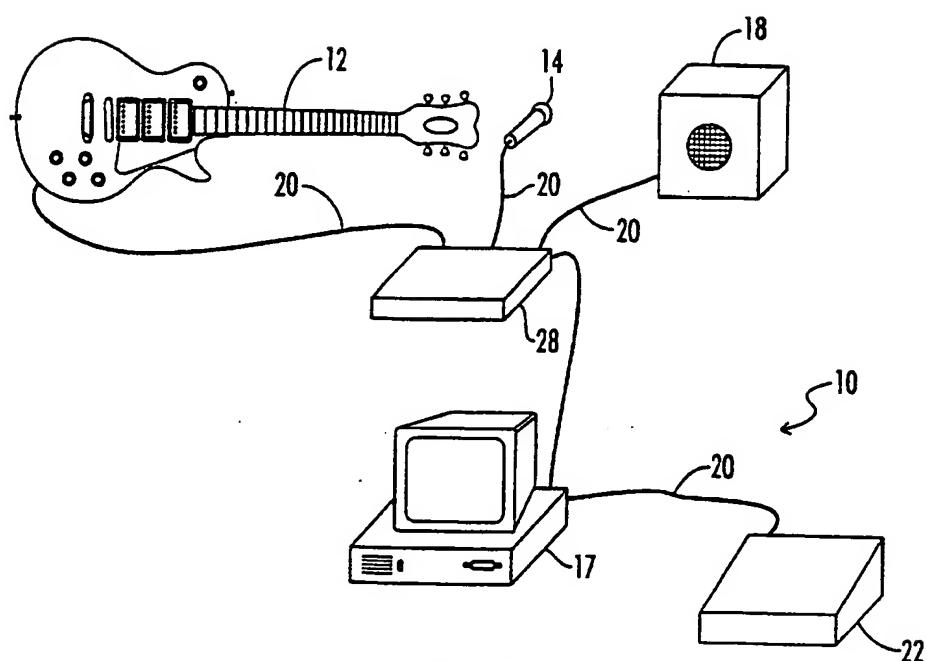


FIG. 1

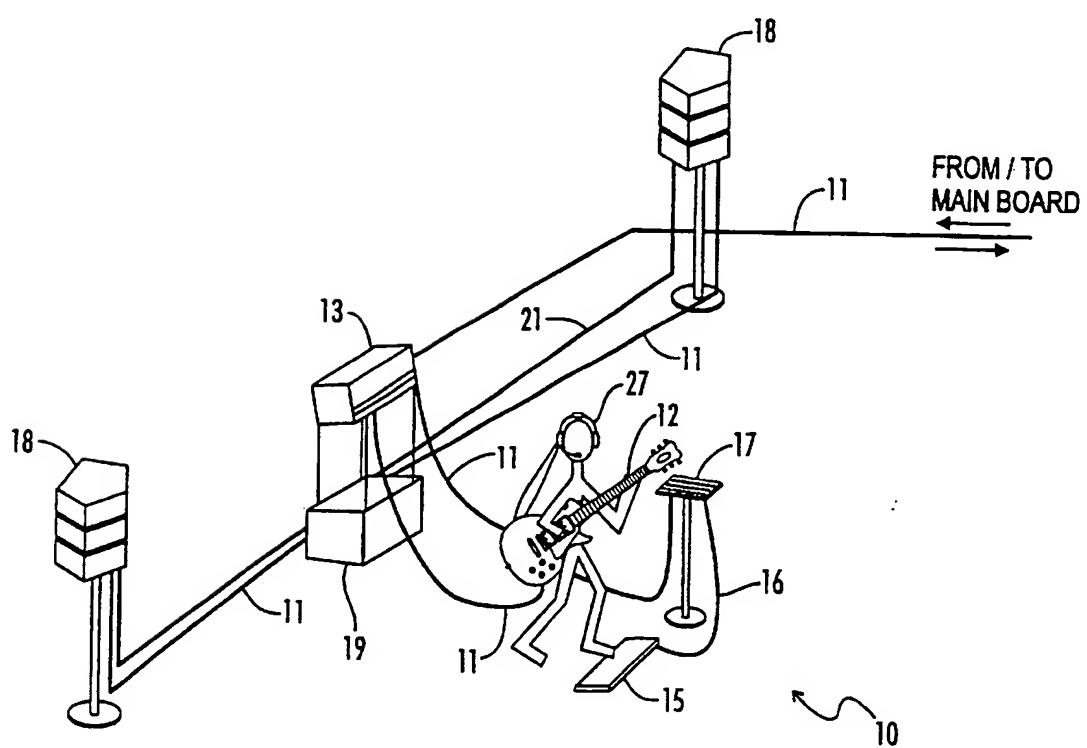


FIG. 2

N9579, N9349, N9350, & N9351
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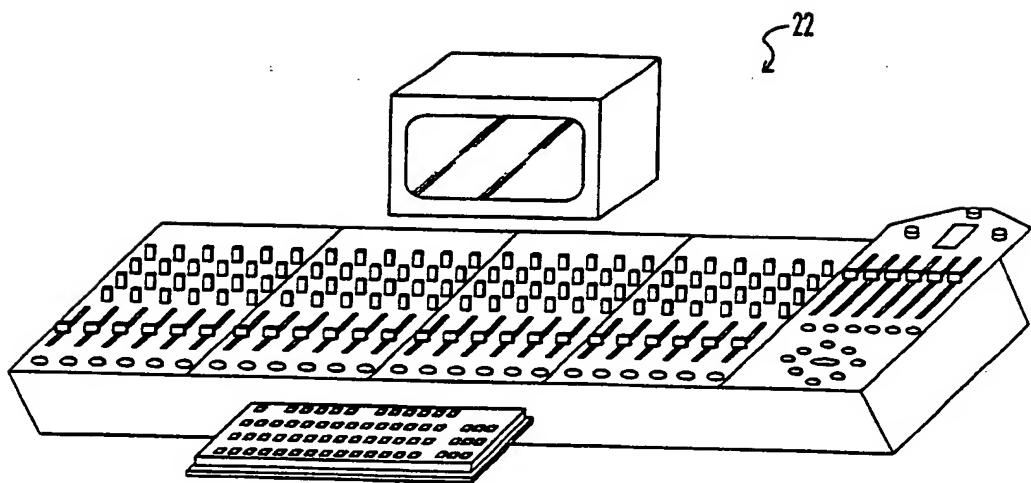


FIG. 3

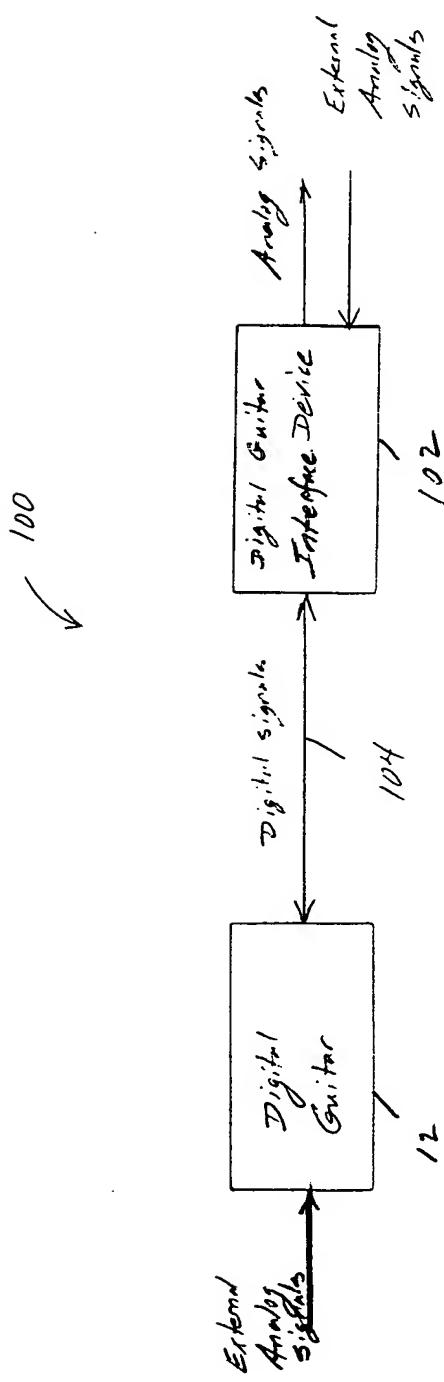


Fig. 4

N9579, N9349, N9350, + N9351
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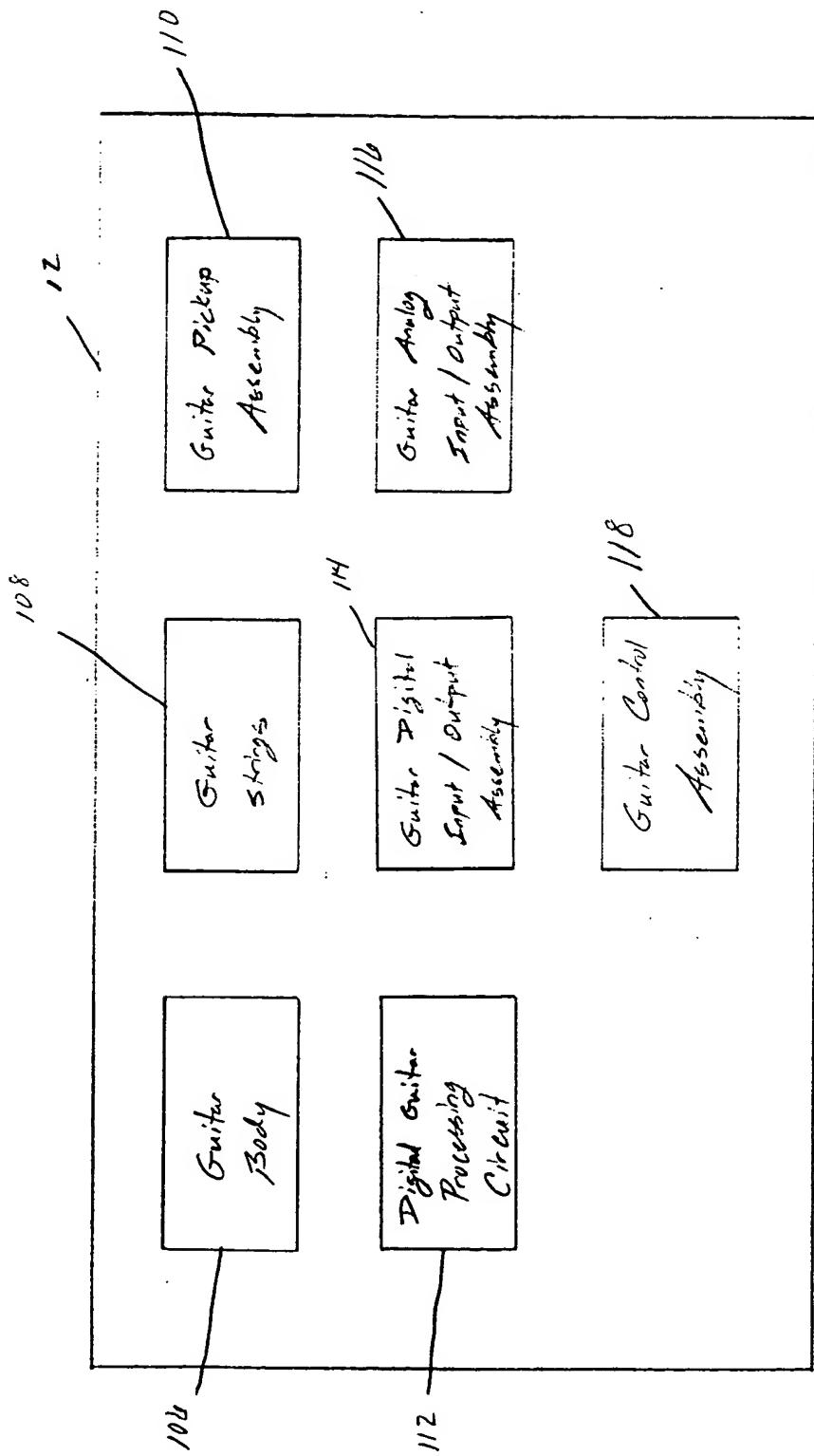


Fig. 5

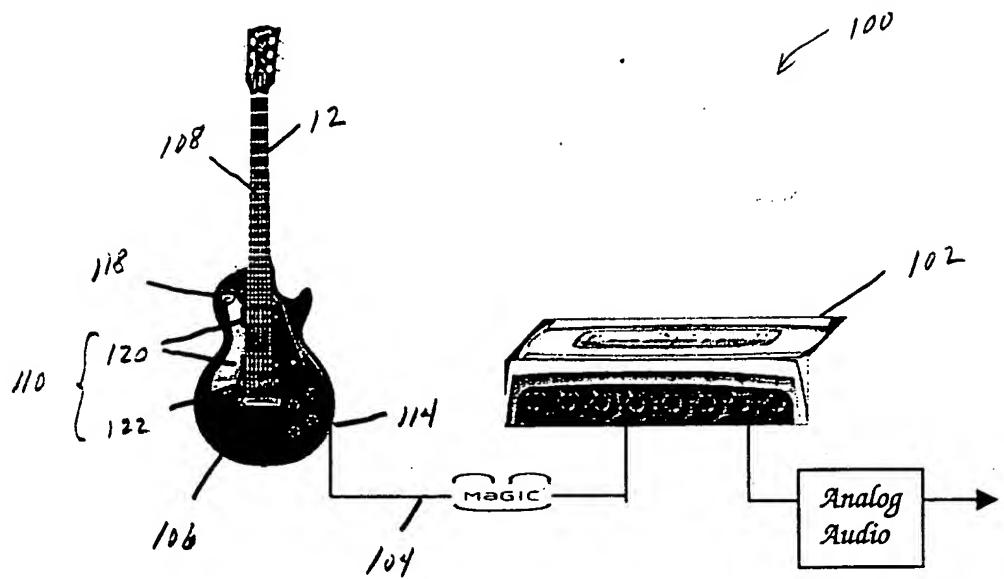


Figure 6

N9579, N9349, N9350 & N9351
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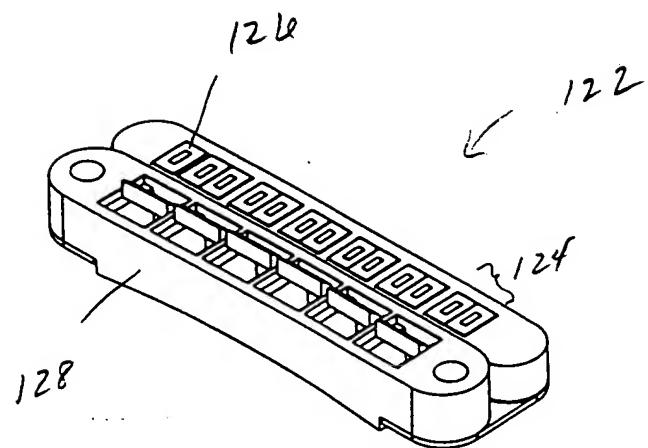
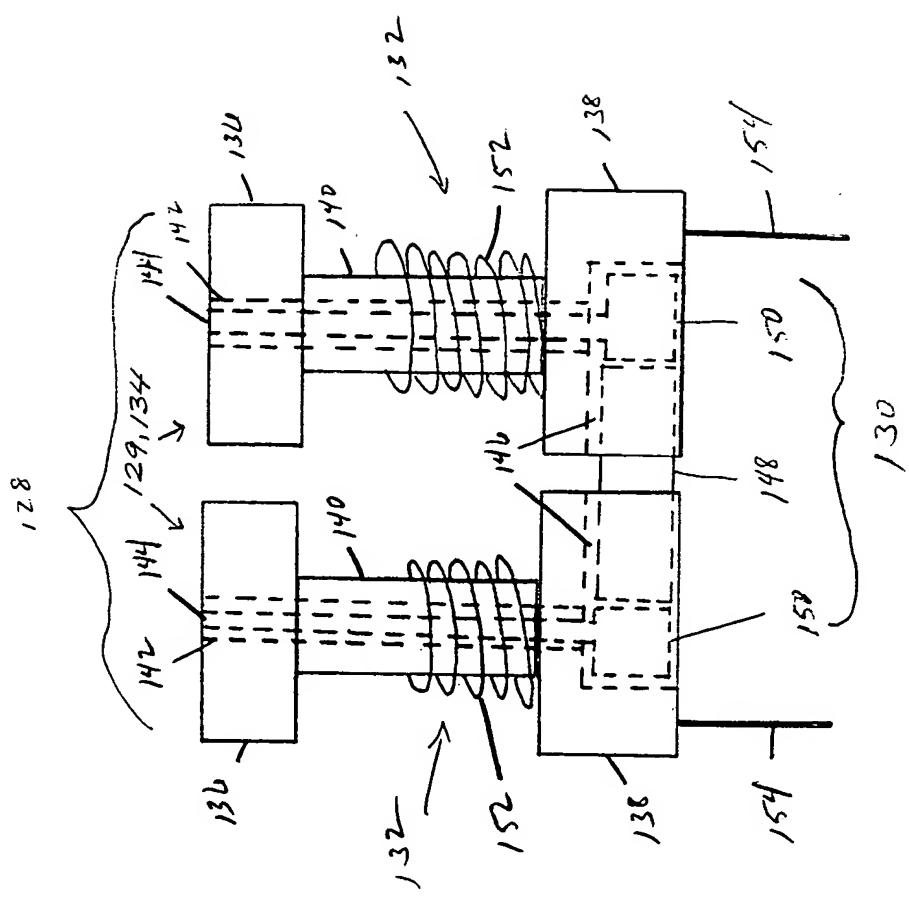


Fig. 7



Digital Guit. Pre-amp. Circuit 112

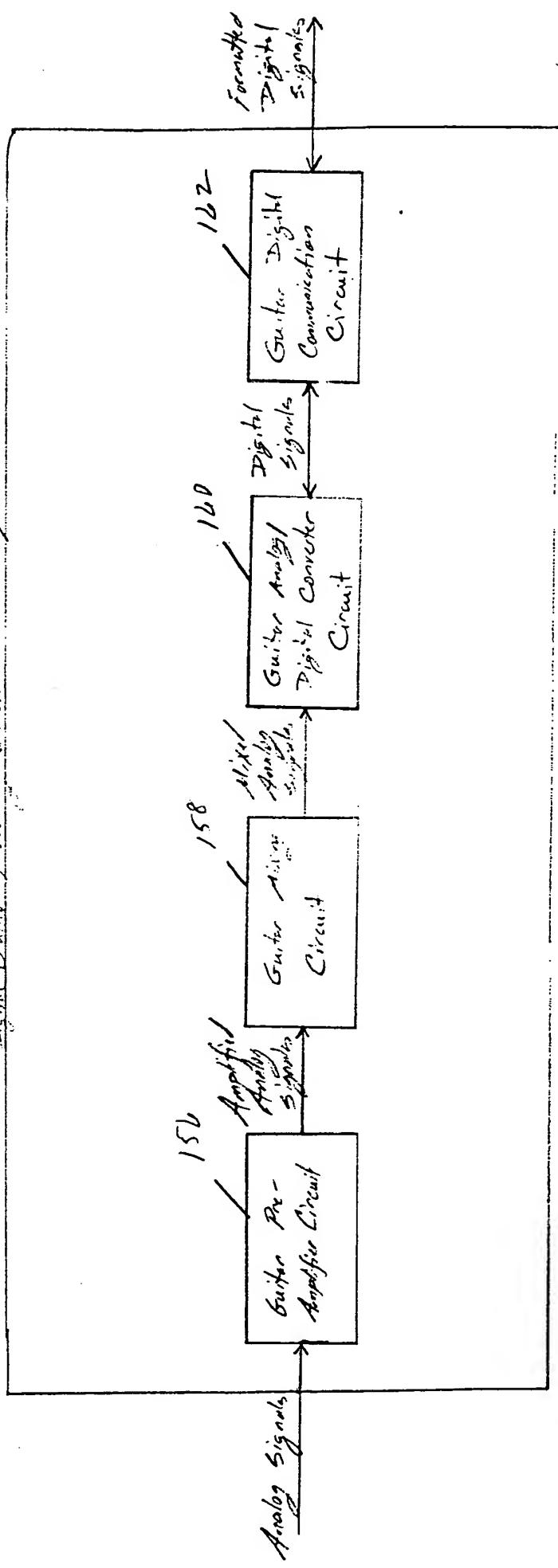


Fig. 9

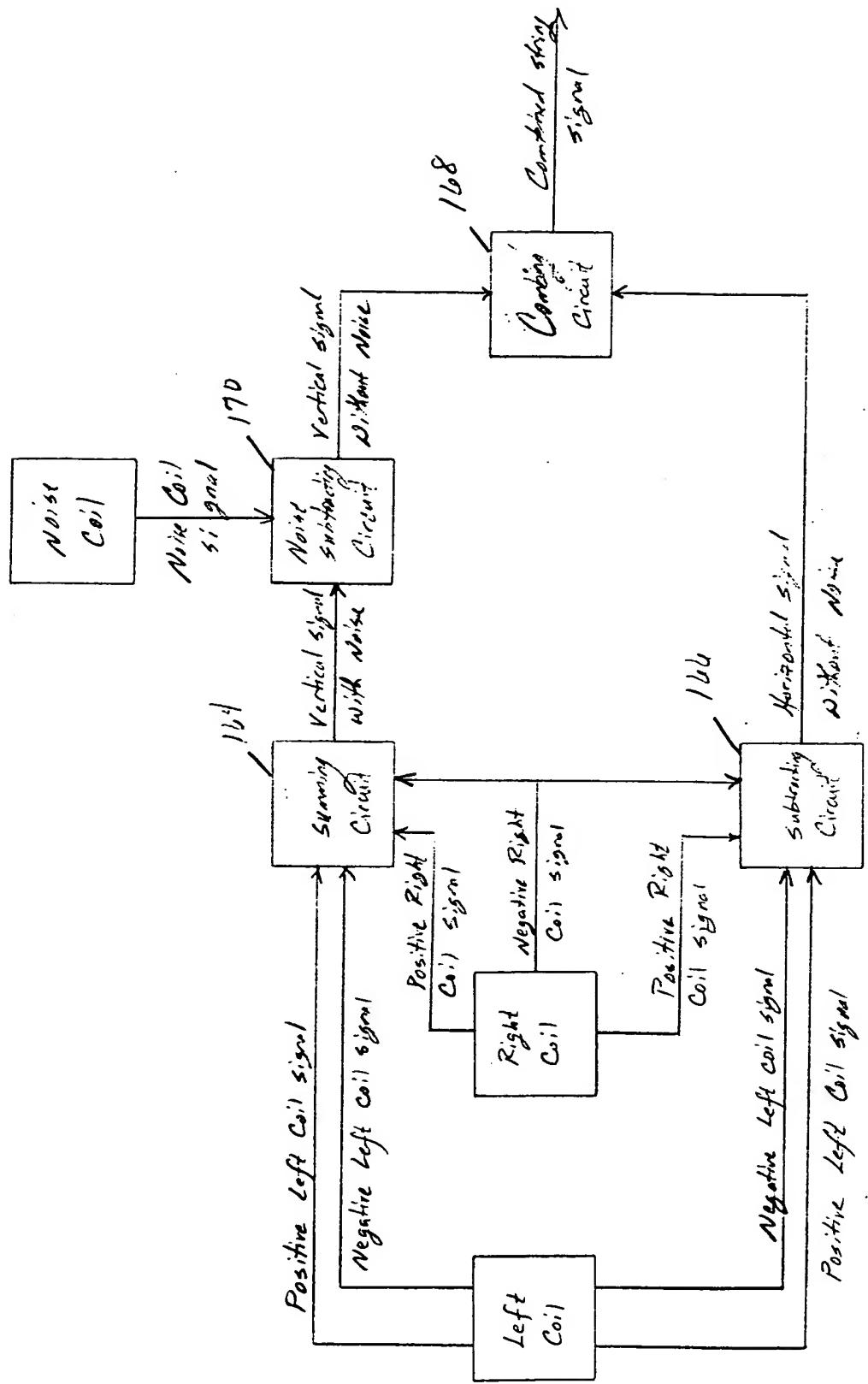


Fig. 10

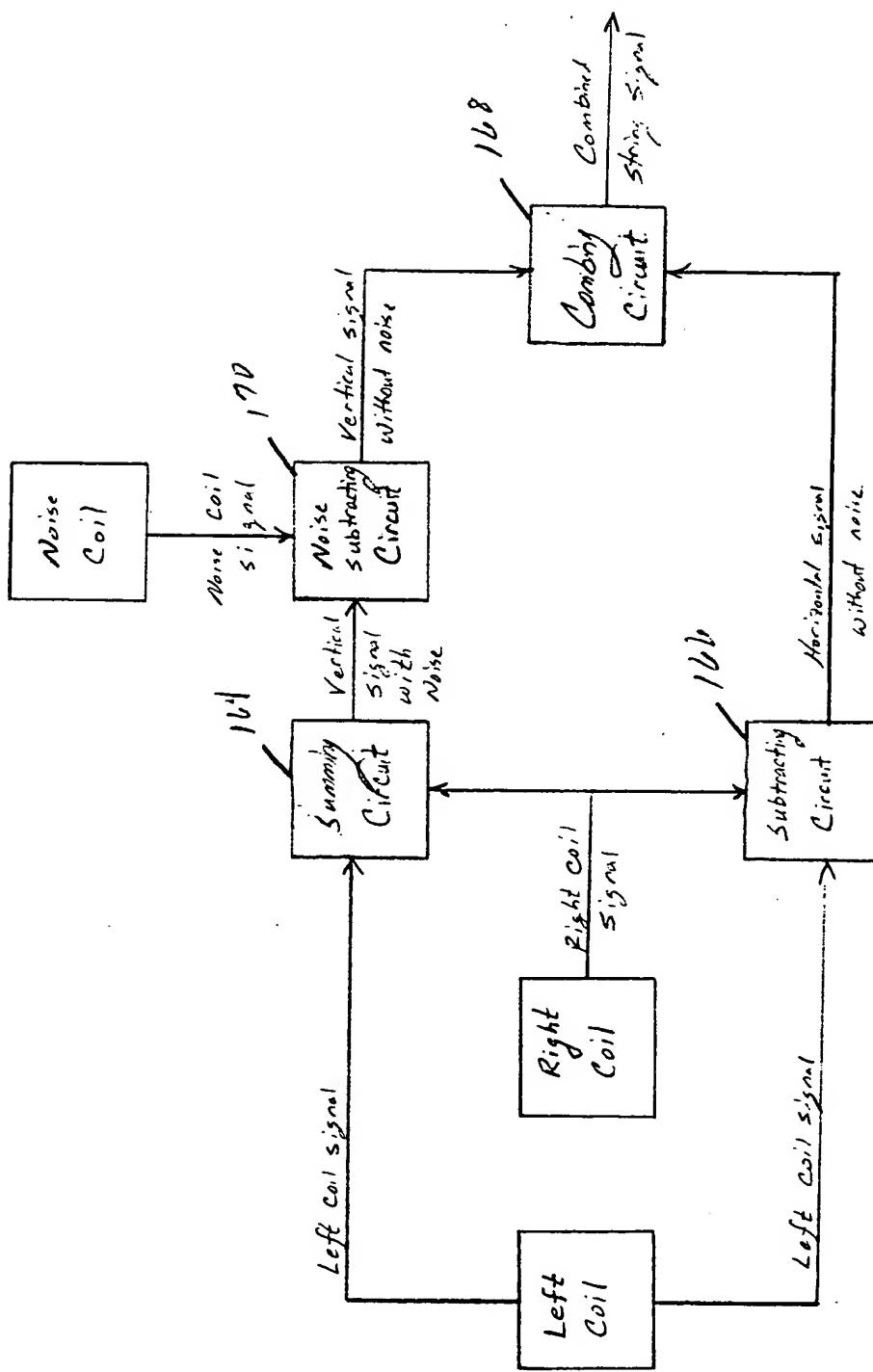


Fig. 11

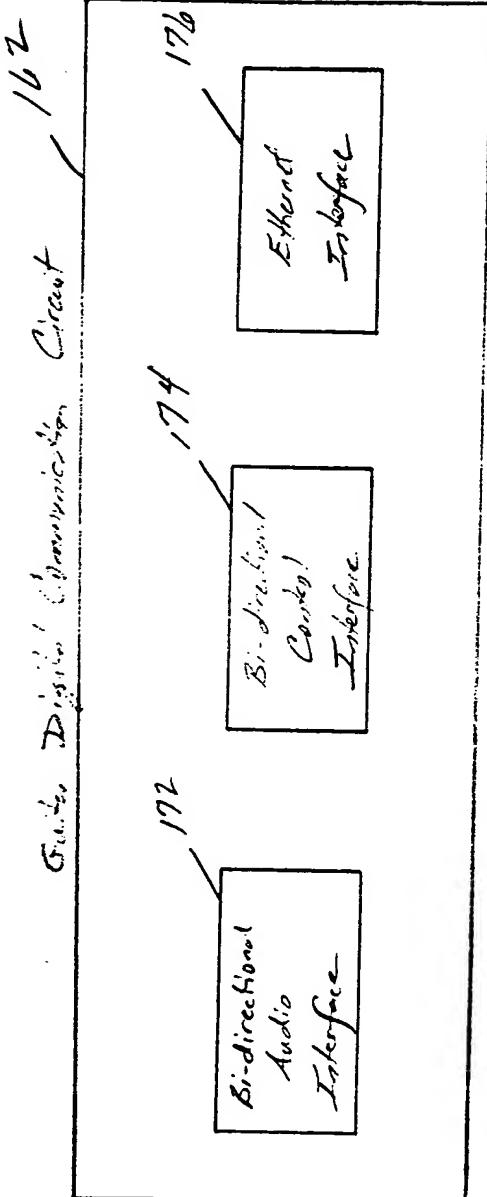


Fig. 12

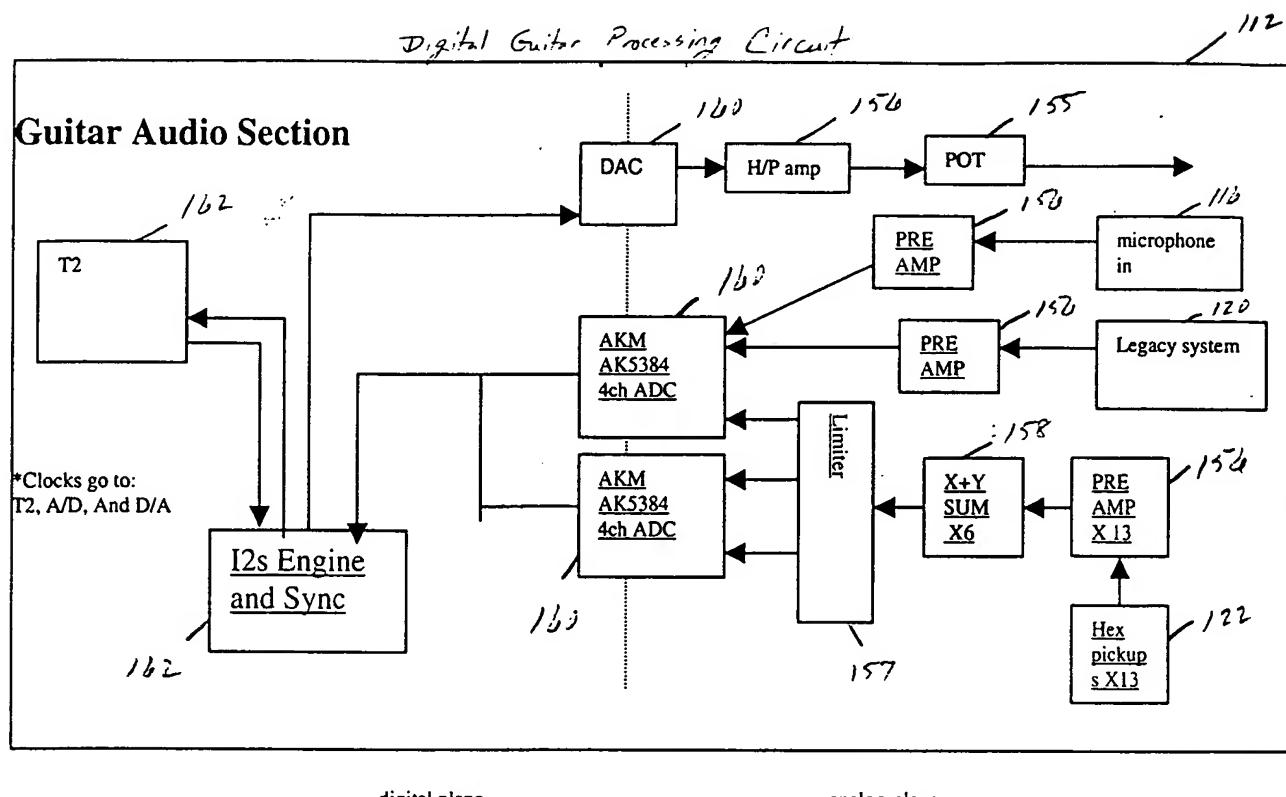


Figure 13

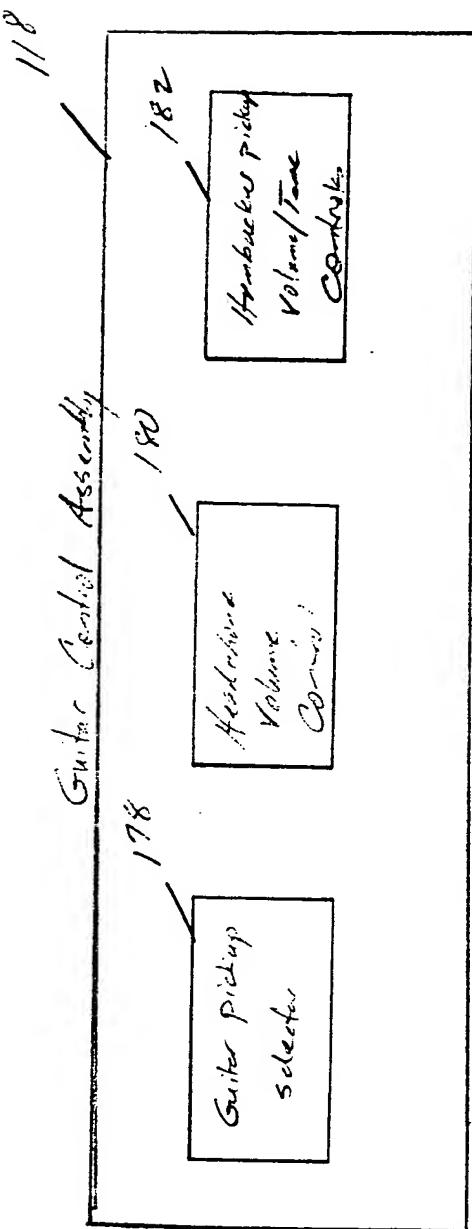


Fig. 118

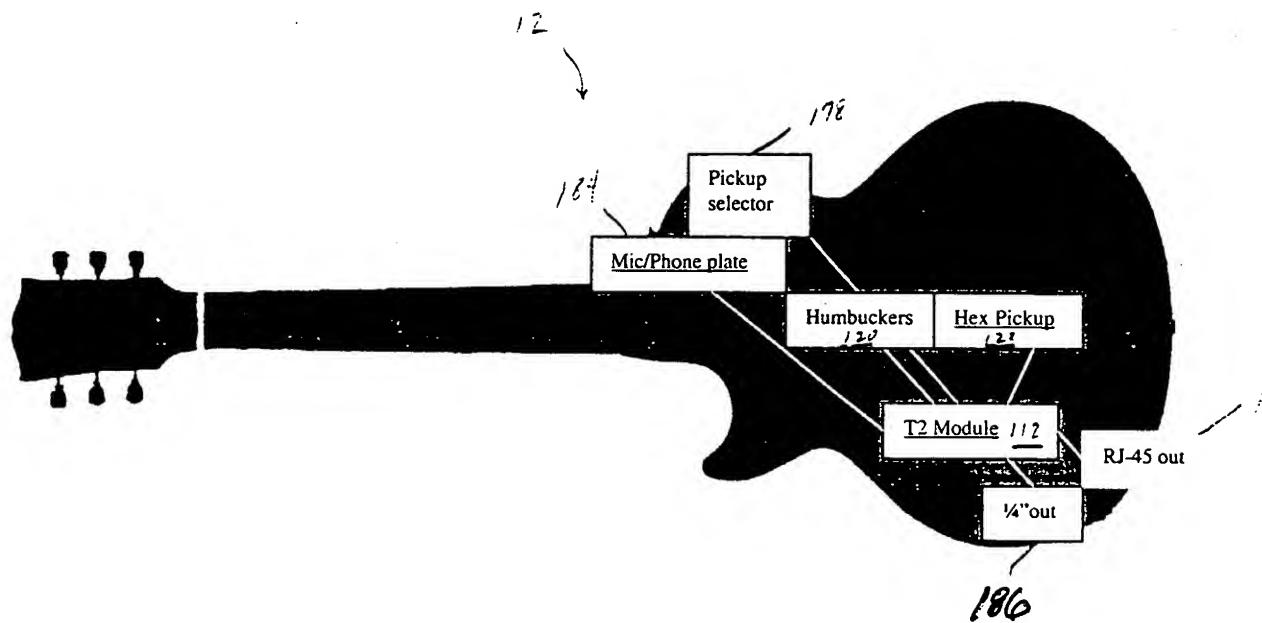
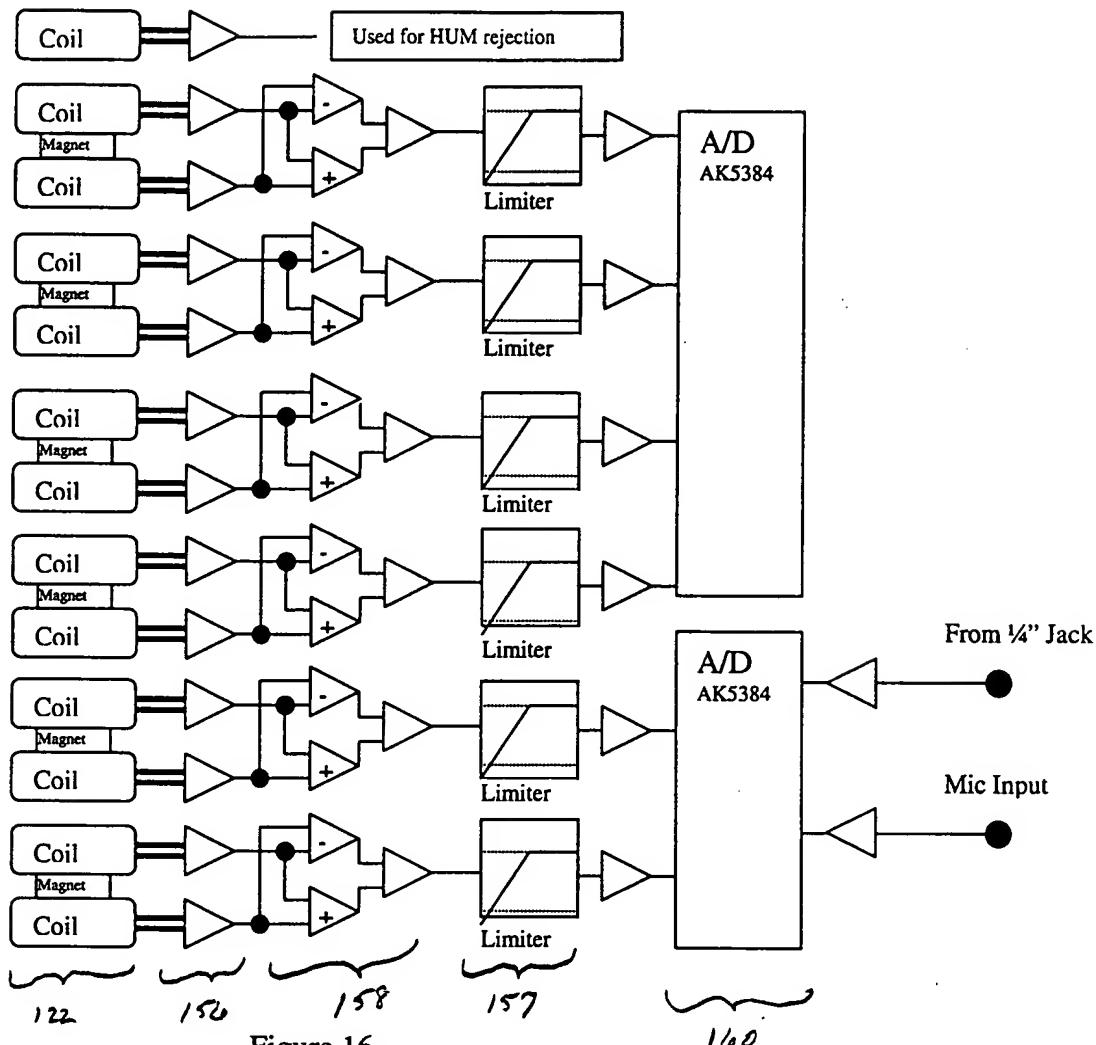


Figure 15

Preamp Section



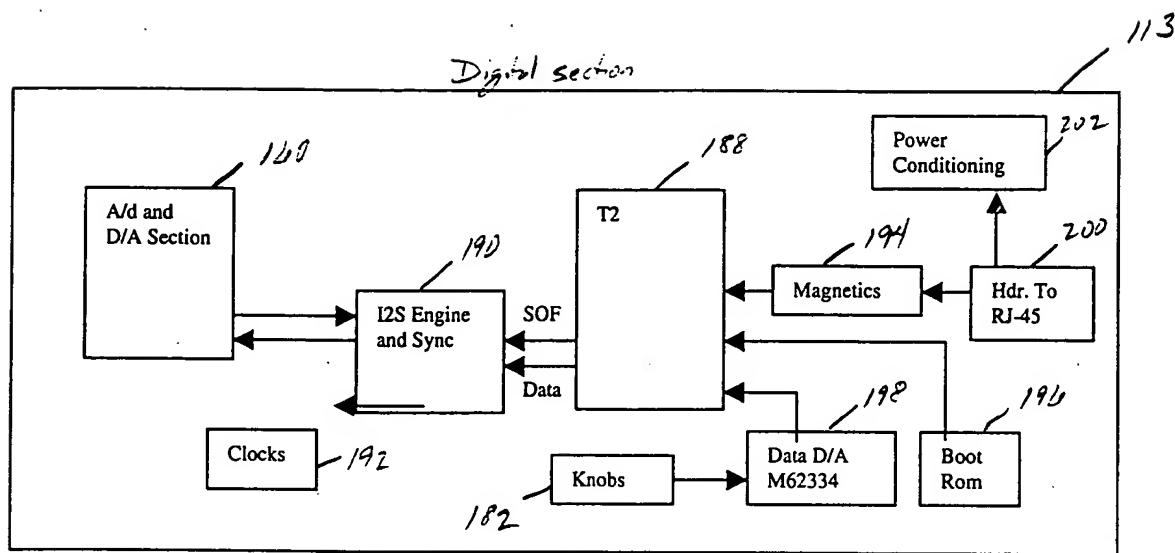


Figure 17

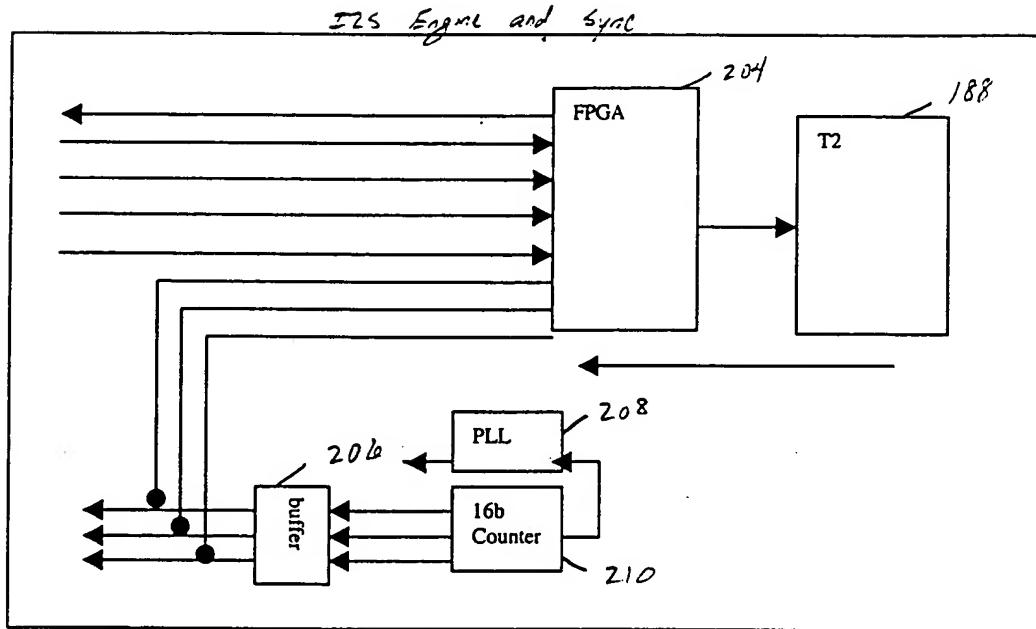


Figure 18

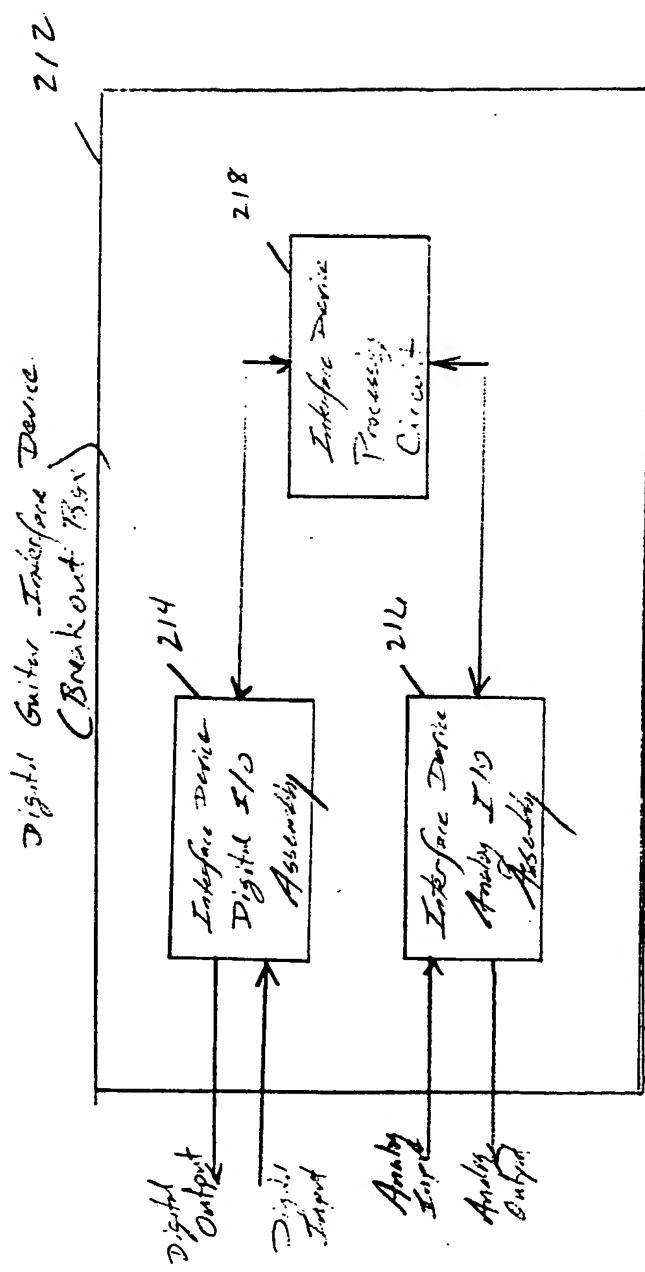


Fig. 19

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Interface Device Processing Circuit

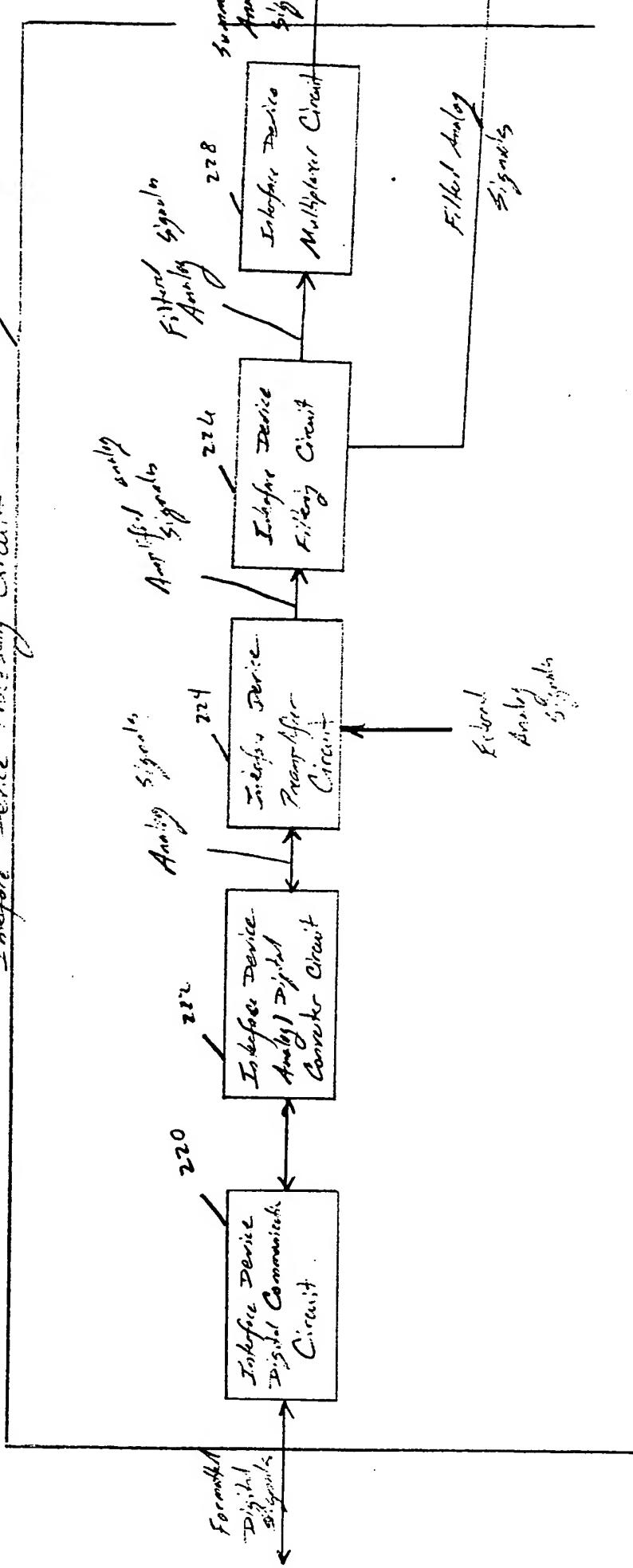
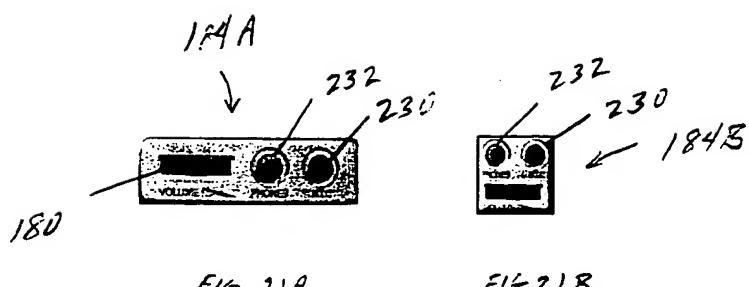
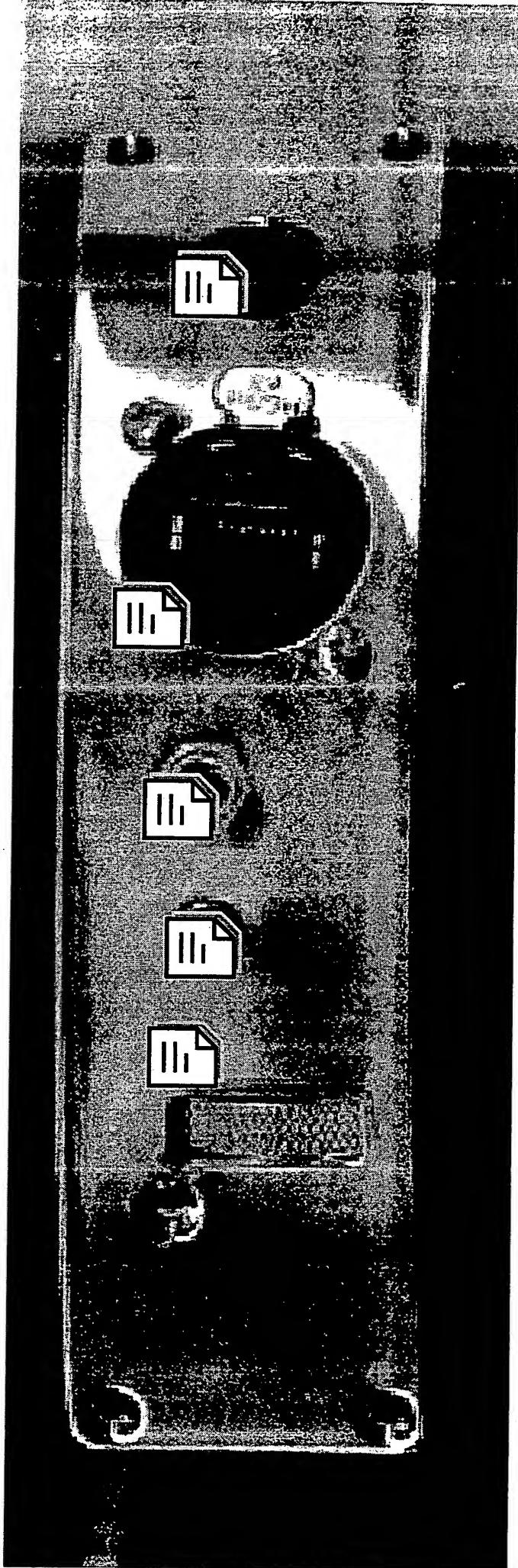


Fig. 20

N9579, N9349, N9350 & N9351
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F16. 21c

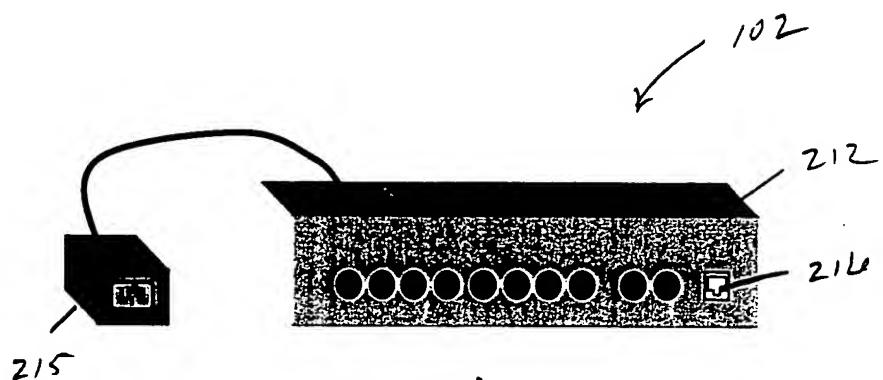


Figure 22 A

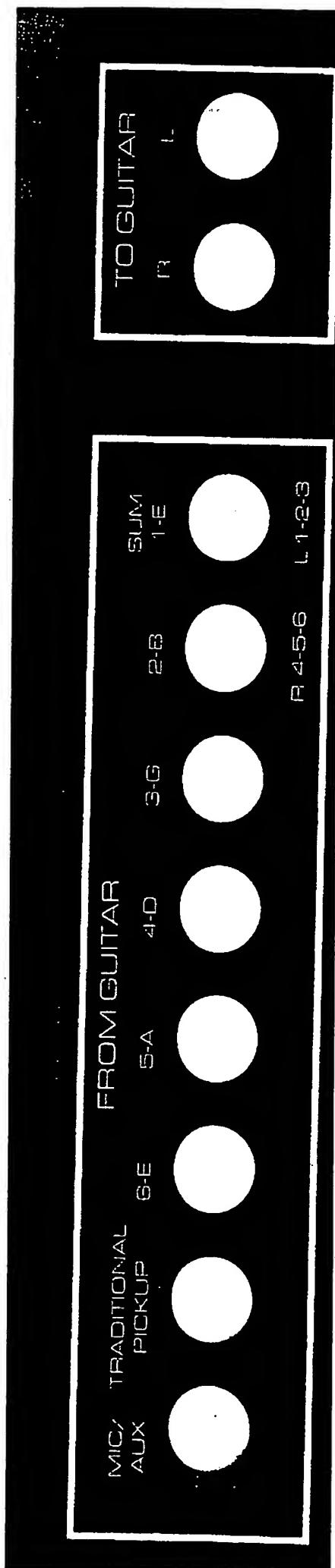


FIG. 22 B

N9579, N9349, N9350 + N9351
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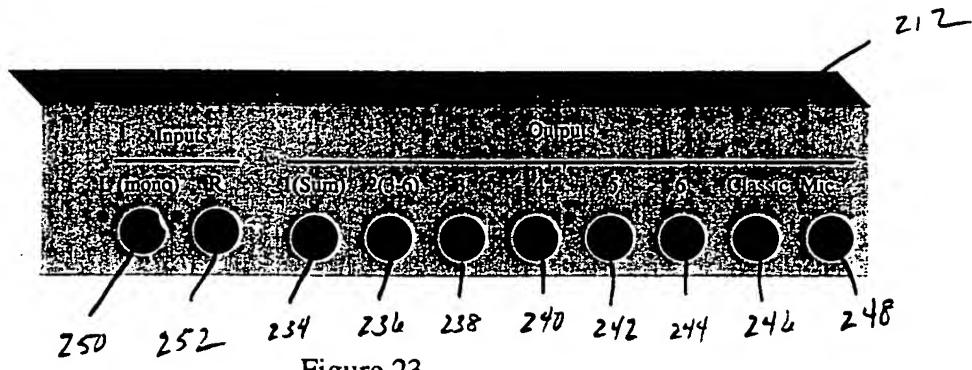


Figure 23

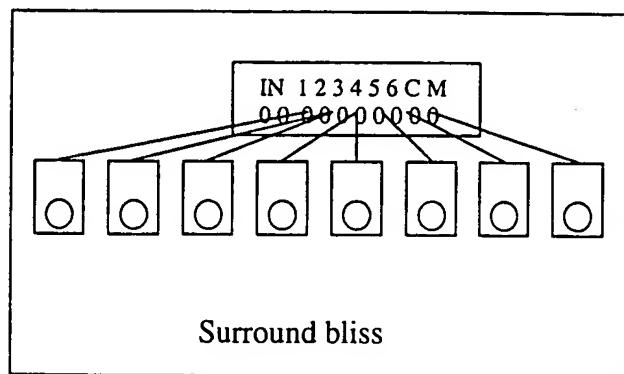
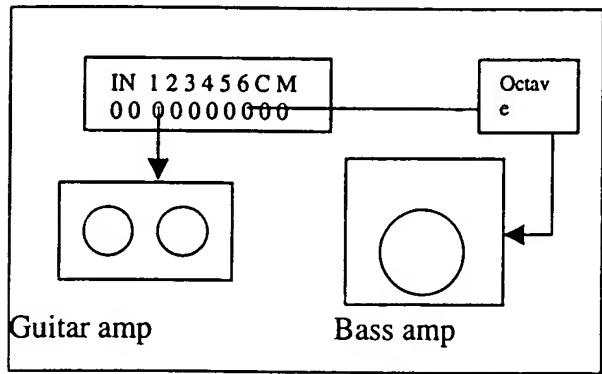
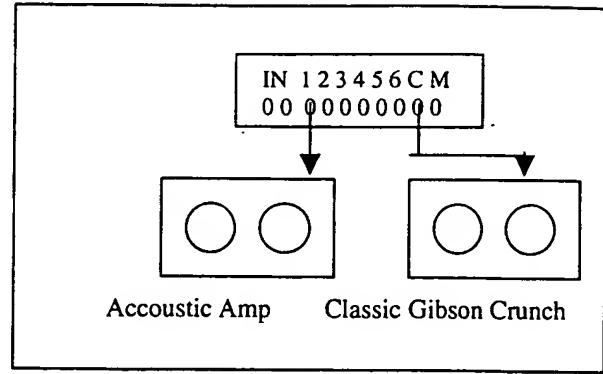
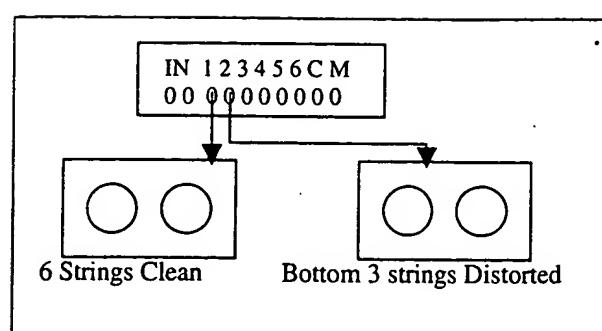


Figure 24

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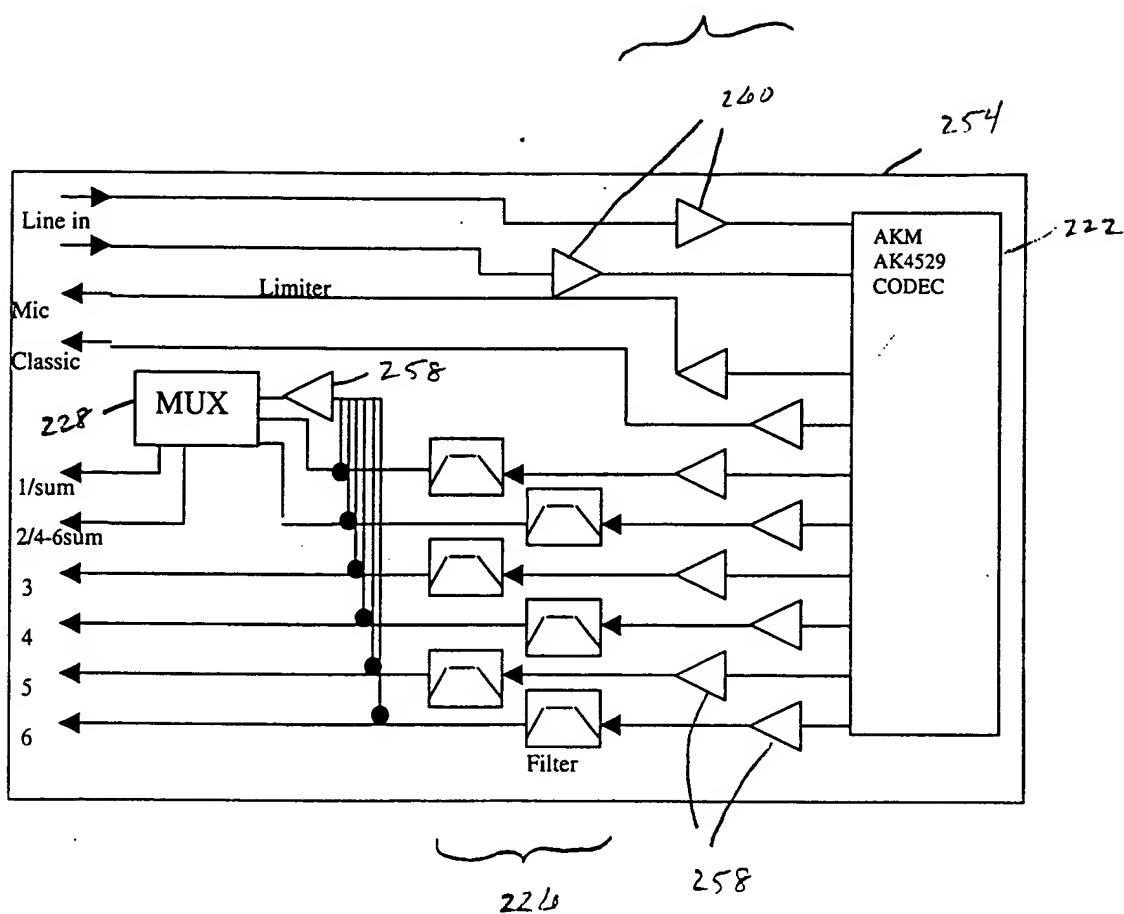


Figure 25

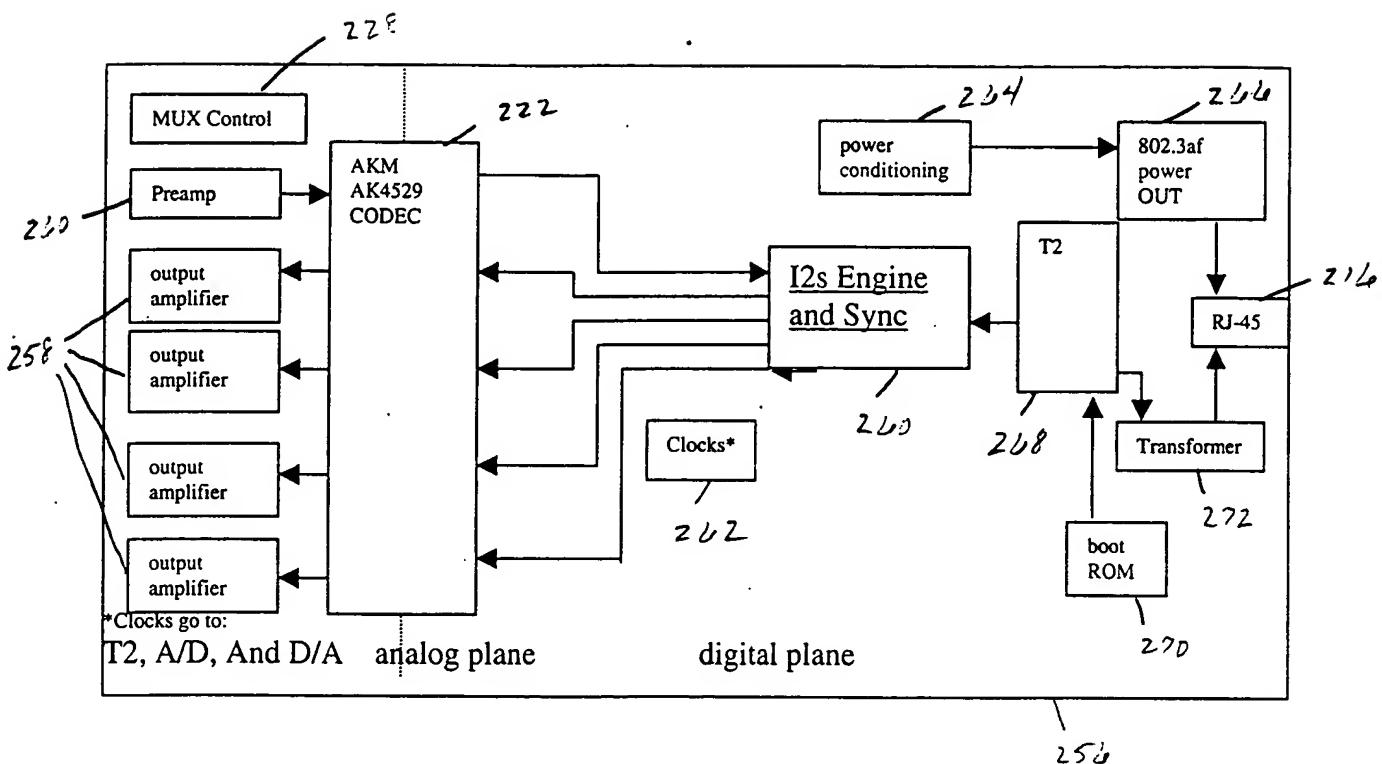


Figure 26

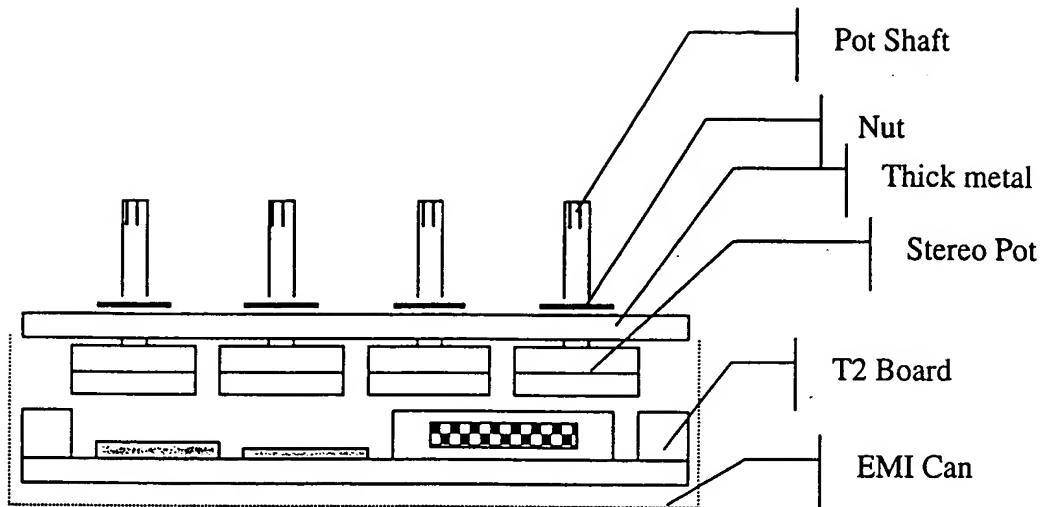


Figure 27

Passive Legacy system and Control Section

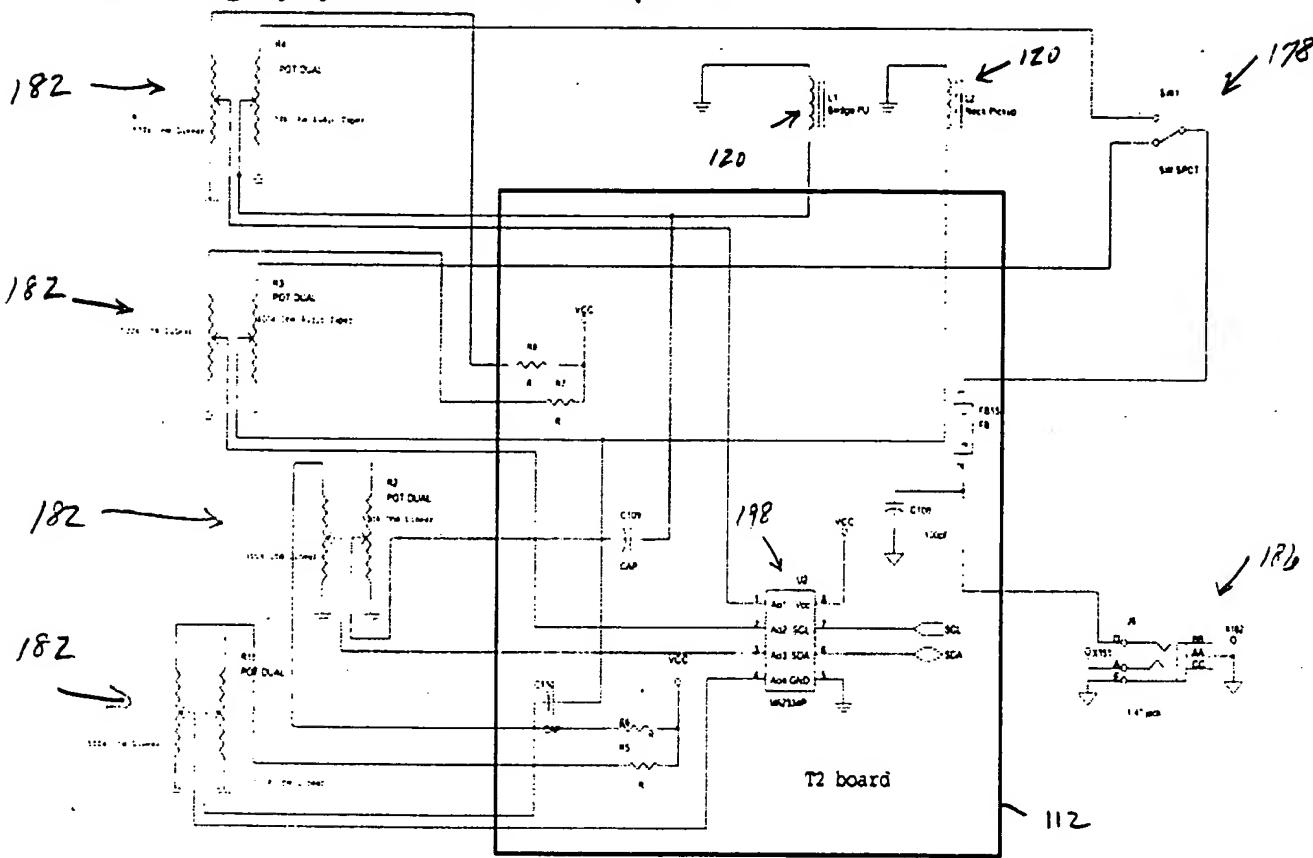
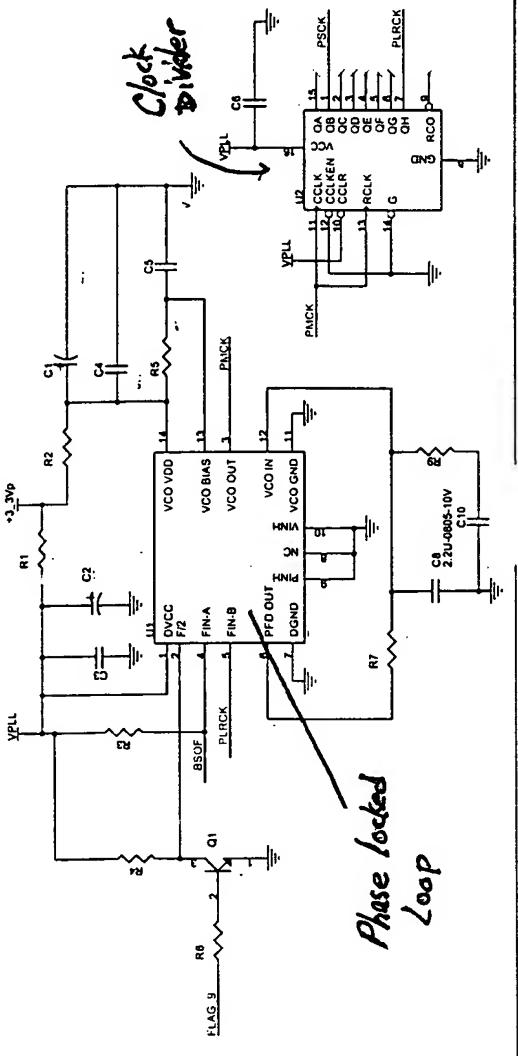
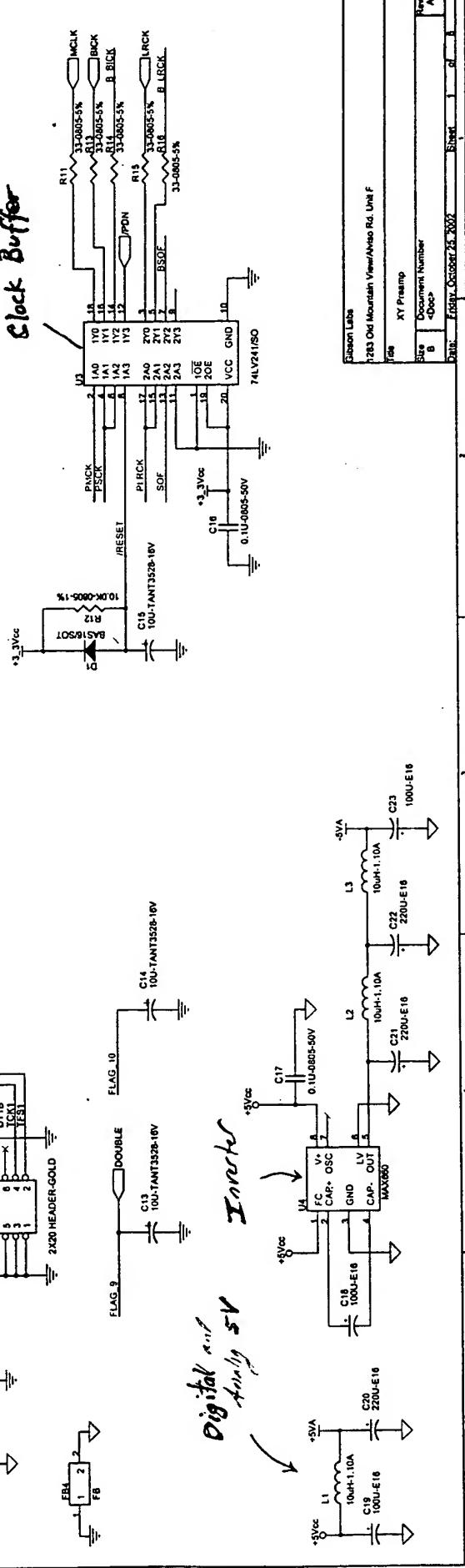


Figure 28

NOTE: All parts within this area powered by VPLL

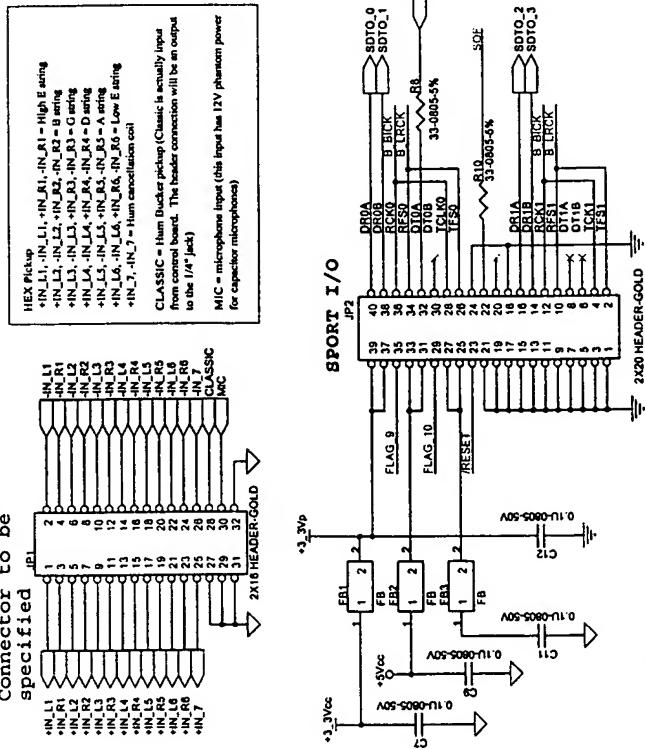


Phase locked
loop



Digital and finally 5G Inverter

Pickup & Mic Inputs
Connector to be
specified



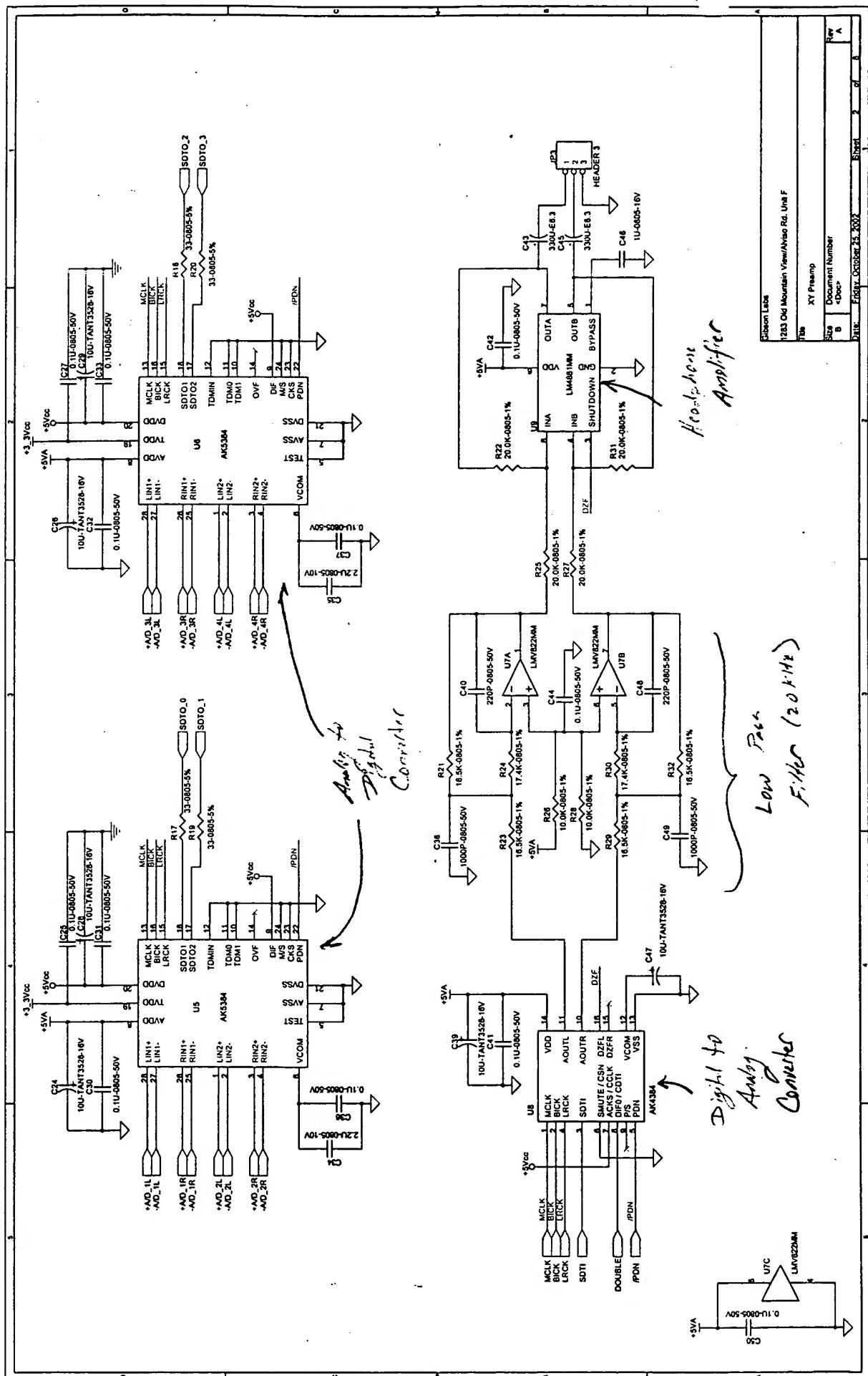
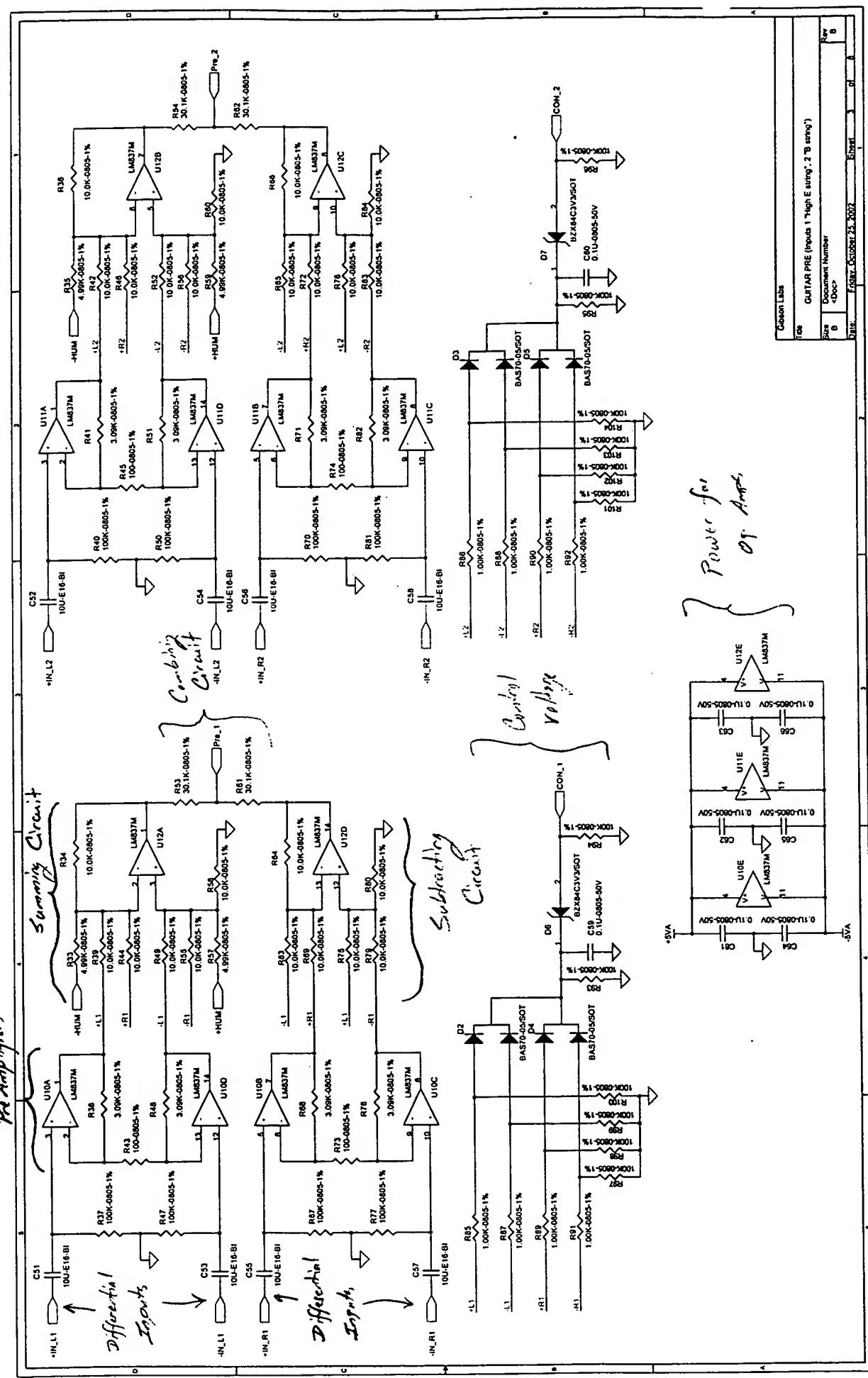
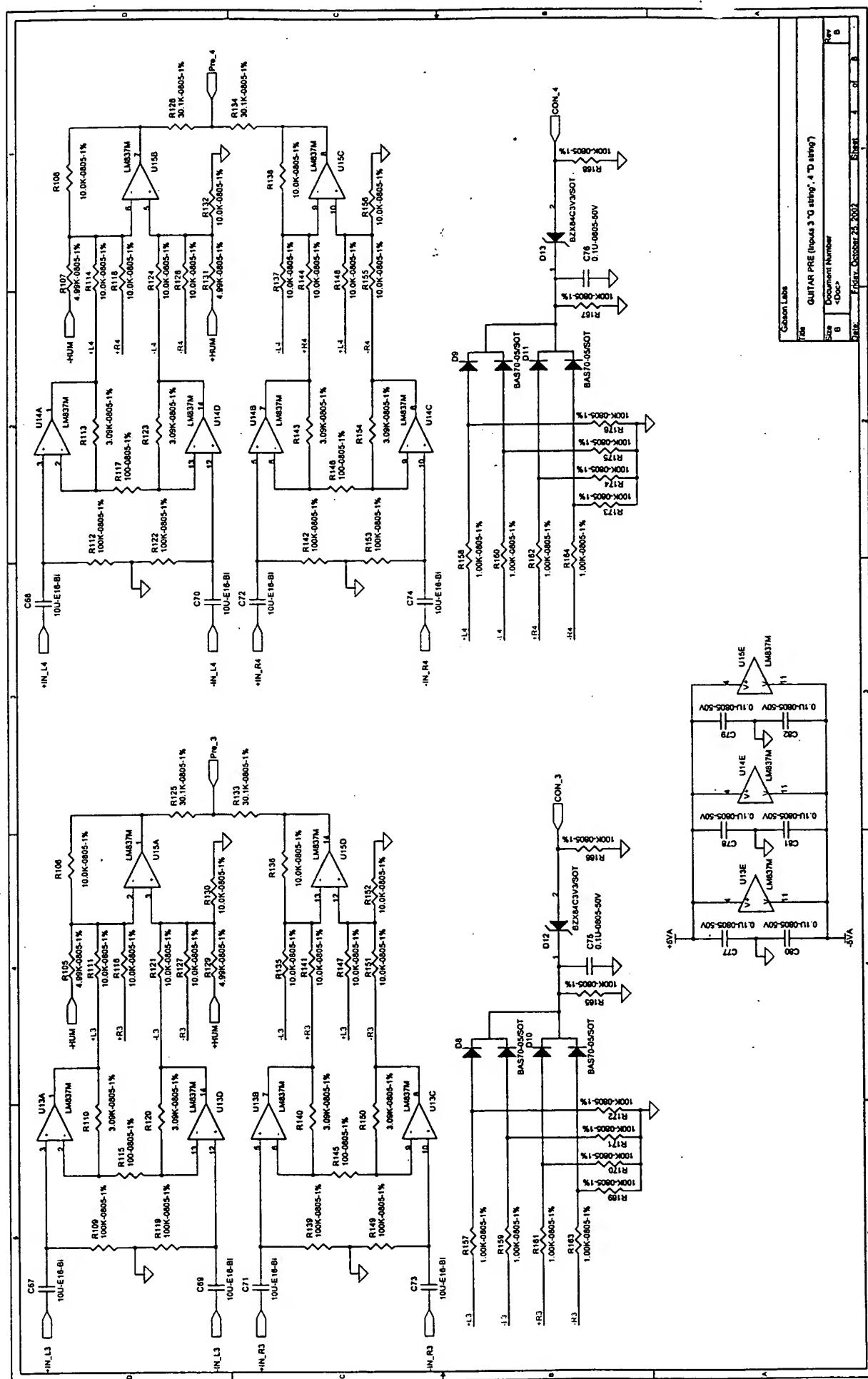
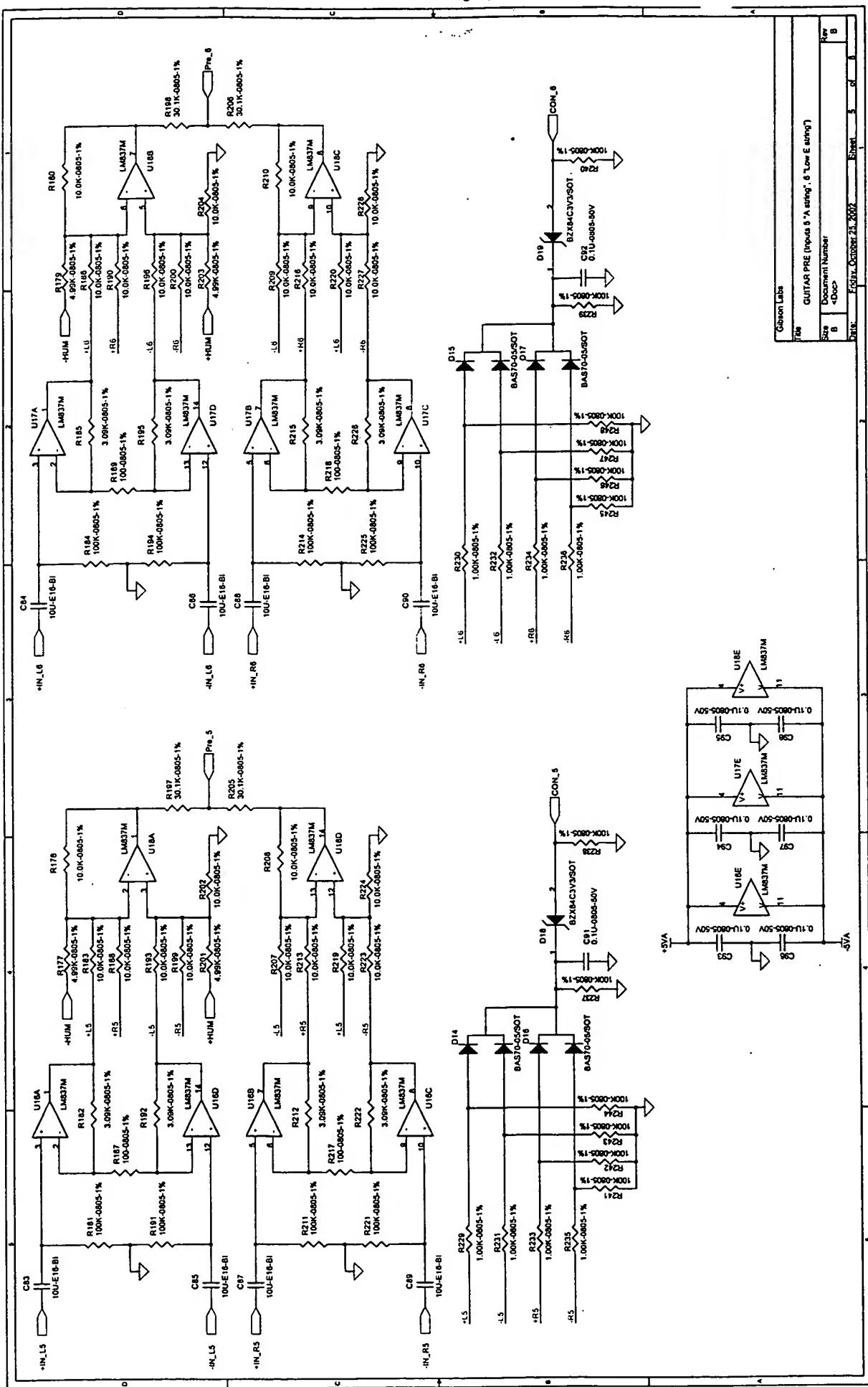


Fig. 30







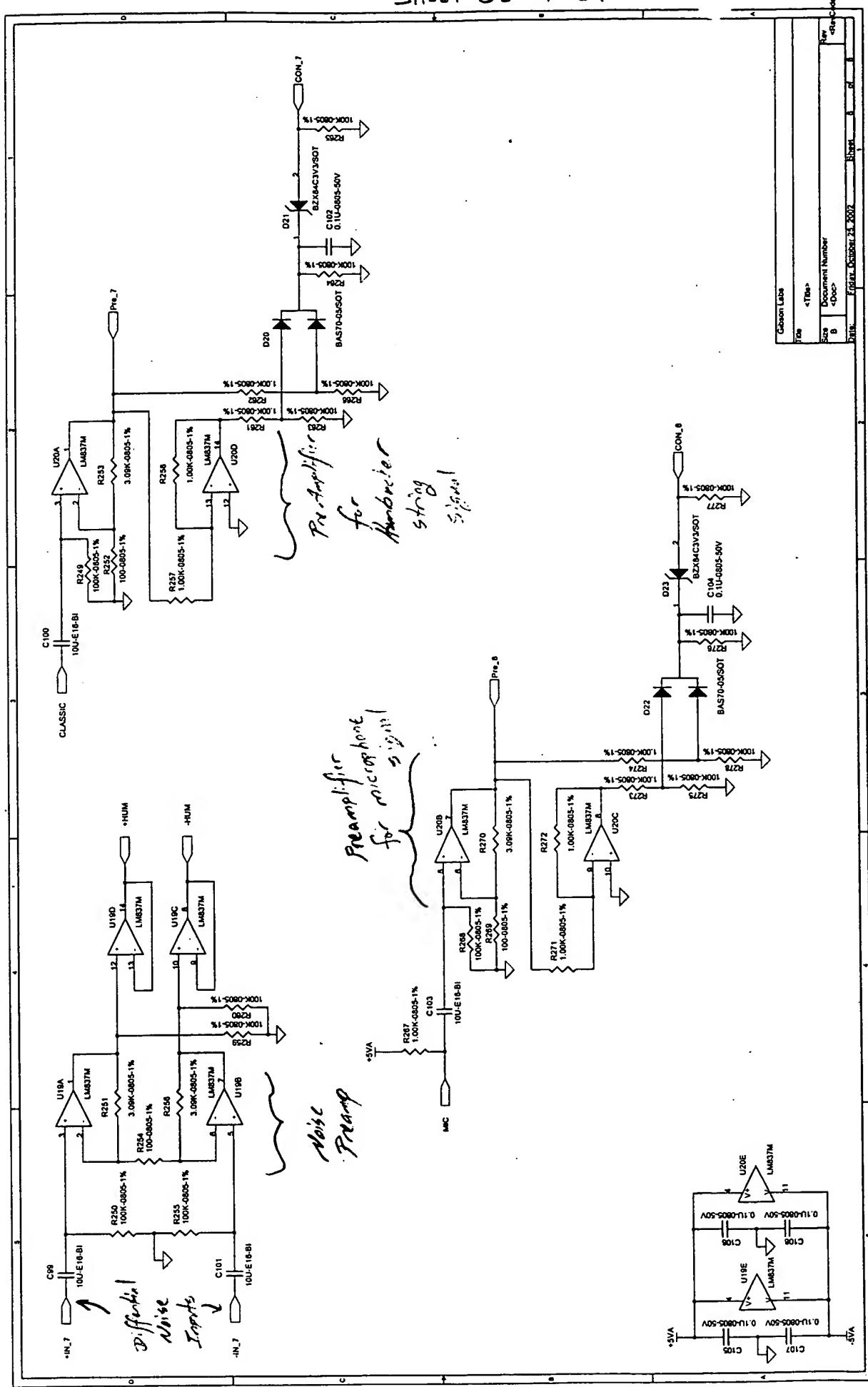


Fig. 34

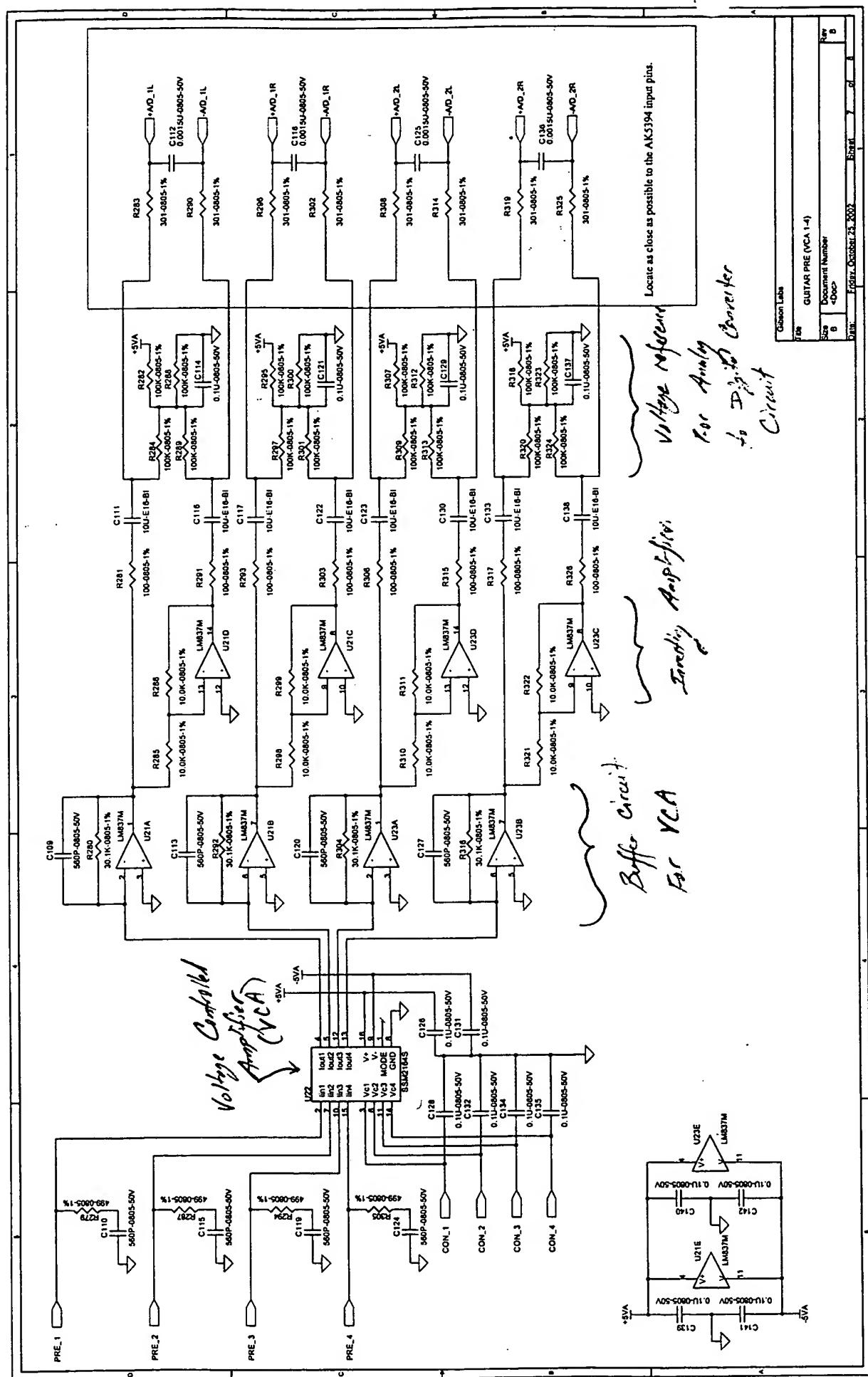


Fig. 35

